Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.041”**

**1**

**7**

**3 2**

**4**

**5**

**6**

**PAD FUNCTION:**

1. **OFFSET NULL**
2. **INPUT-**
3. **INPUT+**
4. **V-**
5. **OFFSET NULL**
6. **OUTPUT**
7. **V+**

**.040”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .003 x .0045”**

**Backside Potential: V-**

**Mask Ref: P4D**

**APPROVED BY: DK DIE SIZE .040” X .041” DATE: 10/7/21**

**MFG: ON SEMI / MOTOROLA THICKNESS .015” P/N: LM741**

**DG 10.1.2**

#### Rev B, 7/1